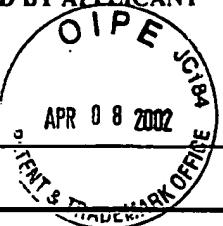


LIST OF REFERENCES CITED BY APPLICANT <i>(Use several sheets if necessary)</i>		ATTY. DOCKET NO.	SERIAL NO.
		100665.0053US1	16/89 942
		APPLICANT	RECEIVED
		Jesse Pedigo, et al.	APR 09 2002
FILING DATE		GROUP	
01/03/02		TC 1700	


U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
YS	3,601,523	08/24/71	Through Hole Connectors	174	68.5	06/19/70
YS	4,106,187	08/15/78	Curved Rigid Printed Circuit Boards	29	625	01/16/76
YS	4,283,243	08/11/81	Use of Photosensitive Stratum to Create Through-Hole Connections in Circuit Boards	156	237	03/20/80
YS	4,360,570	11/23/82	Use of Photosensitive Stratum to Create Through-Hole Connections in Circuit Boards	428	596	06/15/81
YS	4,622,239	11/11/86	Method and Apparatus for Dispensing Viscous Materials	427	96	02/18/86
YS	4,700,474	10/20/87	Apparatus and Method for Temporarily Sealing Holes in Printed Circuit Boards	29	846	11/26/86
YS	4,777,721	10/18/88	Apparatus and Method for Temporarily Sealing Holes in Printed Circuit Boards Utilizing a Thermodeformable Material	29	846	10/15/87
YS	4,783,247	11/8/88	Method and Manufacture for Electrically Insulating Base Material Used in Plated-Through Printed Circuit Panels	204	181.1	05/15/86
YS	4,884,337	12/05/89	Method for Temporarily Sealing Holes in Printed Circuit Boards Utilizing a Thermodeformable Material	29	846	10/15/87
YS	4,954,313	09/04/90	Method and Apparatus for Filling High Density Vias	419	9	02/03/89
YS	4,964,948	10/23/90	Printed Circuit Board Through Hole Technique	156	659	11/13/89
YS	4,995,941	02/26/91	Method of Manufacture Interconnect Device	156	630	05/15/89
YS	5,053,921	10/01/91	Multilayer Interconnect Device and Method of Manufacture Thereof	361	386	10/23/90
YS	5,058,265	10/22/91	Method for Packaging a Board of Electronic Components	29	852	09/10/90
YS	5,117,069	05/26/92	Circuit Board Fabrication	174	261	09/28/90
YS	5,133,120	07/28/92	Method of Filling Conductive Material into Through Holes of Printed Wiring Board	29	852	03/15/91
YS	5,145,691	09/08/92	Apparatus for Packing Filler into Through-Holes or the Like in a Printed Circuit Board	425	110	03/22/91
YS	5,220,723	06/22/93	Process for Preparing Multi-Layer Printed Wiring Board	29	830	11/04/91
YS	5,274,916	01/04/94	Method of Manufacturing Ceramic Multilayer Electronic Component	29	848	12/17/92

LIST OF REFERENCES CITED BY APPLICANT <i>(Use several sheets if necessary)</i>			ATTY. DOCKET NO.	SERIAL NO.
			100665.0053US1	10/039,942
			APPLICANT	
			Jesse Pedigo, et al.	
			FILING DATE	GROUP
			12/20/01	2725
			<i>RECEIVED APR 09 2002 TC 1700</i>	


U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
YS		5,851,344	12/22/98	Ultrasonic Wave Assisted Contact Hole Filling	156	379.6	12/22/98
YS		5,906,042	05/25/99	Method and Structure to Interconnect Traces of Two Conductive Layers in a Printed Circuit Board	29	852	10/04/95
YS		5,925,414	07/20/99	Nozzle and Method for Extruding Conductive Paste into High Aspect Ratio Openings	427	282	07/20/99
YS		5,994,779	11/30/99	Semiconductor Fabrication Employing a Spacer Metallization Technique	257	773	05/02/97
YS		6,000,129	12/14/99	Process for Manufacturing a Circuit with Filled Holes	29	852	03/12/98
YS		6,009,620	01/04/00	Method of Making a Printed Circuit Board Having Filled Holes	29	852	07/15/98
YS		6,079,100	06/27/00	Method of Making a Printed Circuit Board Having Filled Holes and Fill Member for Use Therewith	29	852	05/12/98
YS		6,090,474	07/18/00	Flowable Compositions and Use in Filling Vias and Plated Through-Holes	428	209	07/18/00
YS		6,015,520	01/18/00	Method for Filling Holes in Printed Wiring Boards	264	104	05/15/97
YS		6,106,891	08/22/00	Via Fill Compositions for Direct Attach of Devices and Method for Applying Same	427	97	12/18/98
YS		6,138,350	10/31/00	Process for Manufacturing a Circuit Board with Filled Holes	29	852	02/25/98
YS		6,149,857	11/21/00	Method of Making Films and Coatings Having Anisotropic Conductive Pathways Therein	264	429	12/22/98
YS		6,153,508	11/28/00	Multi-Layer Circuit Having a Via Matrix Interlayer Connection and Method for Fabricating the Same	438	622	02/19/98
YS		6,184,133	02/06/01	Method of Forming an Assembly Board with Insulator Filled Through Holes	438	667	02/18/00
YS		6,261,501	07/17/01	Resin Sealing Method for A Semiconductor Device	264	272.15	01/22/99
YS		6,276,055	08/21/01	Method and Apparatus for Forming Plugs in Vias of a Circuit Board Layer	29	852	09/24/98
YS		6,281,448	08/28/01	Printed Circuit Board and Electronic Components	174	260	08/10/99
YS		6,282,782	09/04/01	Forming Plugs in Vias of Circuit Board Layers and Subassemblies	29	852	09/02/99

Y S	5,277,854	01/11/94	Methods and Apparatus for Making Grids from Fibers	264	86	06/06/91
Y S APR 8 2002	5,332,439	07/26/94	Screen Printing Apparatus for Filling Through-Holes in Circuit Board with Paste	118	213	08/18/92
Y S	5,340,779	07/30/96	Apparatus for Manufacture of Multi-Layer Ceramic Interconnect Structures	118	692	03/01/95
Y S	5,766,670	06/16/98	Via Fill Compositions for Direct Attach of Devices and Methods for Applying Same	427	8	11/17/93
Y S	5,578,151	11/26/96	Manufacture of A Multi-Layer Interconnect Structure	156	64	03/01/95
Y S	5,591,353	01/07/97	Reduction of Surface Copper Thickness on Surface Mount Printed Wire Boards with Copper Plated Through Holes by the Chemical Planarization Method	216	18	08/18/94
Y S	5,610,103	03/11/97	Ultrasonic Wave Assisted Contact Hole Filling	437	225	12/12/95
Y S	5,637,834	06/10/97	Multilayer Circuit Substrate and Method for Forming Same	174	264	02/03/95
Y S	5,662,987	09/02/97	Multilayer Printed Wiring Board and Method of Making Same	428	209	02/01/96
Y S	5,699,613	12/23/97	Fine Dimension Stacked Vias for a Multiple Layer Circuit Board Structure	29	852	09/25/95
Y S	5,707,575	01/13/98	Method for Filling Vias in Ceramic Substrates with Composite Metallic Paste	264	104	07/28/94
Y S	5,744,171	04/28/98	System for Fabricating Conductive Epoxy Grid Array Semiconductor Packages	425	110	05/12/97
Y S	5,744,285	04/28/98	Composition and Process for Filling Vias	430	318	07/18/96
Y S	5,753,976	05/19/98	Multi-Layer Circuit Having a Via Matrix Interlayer Connection	257	774	06/14/96
Y S	5,761,803	06/09/98	Method of Forming Plugs in Vias of A Circuit Board by Utilizing a Porous Membrane	29	852	06/26/96
Y S	5,766,670	06/16/98	Via Fill Compositions for Direct Attach of Devices and Methods for Applying Same	427	8	11/17/93
Y S	5,822,856	10/20/98	Manufacturing Circuit Boards Assemblies Having Filled Vias	29	832	06/28/96
Y S	5,824,155	10/20/98	Method and Apparatus for Dispensing Viscous Material	118	410	11/08/95

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

		RECEIVED APR 9 2002
		TO 1700

EXAMINER Yuey Leeeeetko	DATE CONSIDERED 02/24/2005
----------------------------	-------------------------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

LIST OF REFERENCES CITED BY APPLICANT <i>(Use several sheets if necessary)</i>		ATTY. DOCKET NO.	SERIAL NO.
		100665.0053US1	10/039,942
		APPLICANT	
		Jesse Pedigo, et al.	
		FILING DATE	GROUP
		January 3, 2002	1725


U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
YS		5,277,854	01/11/94	Hunt	264	86	06/06/91
YS		5,451,721	09/19/95	Tsukada, et al.	17	261	09/24/91
YS		5,456,004	10/10/95	Swamy	29	862	01/04/94
YS		5,471,091	11/28/95	Pasch, et al.	257	752	08/26/91
YS		5,532,516	07/02/96	Pasch, et al.	257	752	03/28/95
YS		5,753,976	05/19/98	Harvey	257	774	06/14/96

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
					YES	NO	
YS		WO 00/13474					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER			DATE CONSIDERED
Yuriy Selleen NO			12/09/2004

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FOREIGN PATENT DOCUMENTS

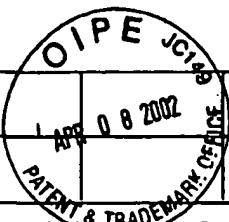
O I P E S C I E N C E P A T E N T T R A D E M A R K S E R V I C E Y S	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
Y S	EP 0 194 247 A2	APR 08 2002				V	
Y S	EP 0 713 358 A2					V	
Y S	EP 0 723 388 A1					V	
Y S	GB 2 120 017 A					V	
Y S	GB 2 341 347 A					V	
Y S	GB 2 246 912 A					V	
Y S	JP 04239193					V	
Y S	JP 05275819					V	
Y S	JP 53-104857					V	
Y S	JP 54-139065					V	
Y S	JP 62-277794					V	
Y S	JP 62-287696					V	
Y S	JP 03004595					V	
Y S	JP 04186792					V	
Y S	JP 07176871					V	
Y S	JP 08172265					V	
Y S	JP 08191184					V	
Y S	JP 09321399					V	
Y S	JP 09083135					V	
Y S	JP 10065339					V	
Y S	JP 10256687					V	
	JP 11054909						
Y S	JP 1173696					V	
Y S	JP 1236694						V
Y S	JP 58011172					V	
Y S	FR 2 684 836						V

RECEIVED

APR 09 2002

TC 1700

VS		FR 2 714 567								V
VS		WO 86/06243								V



OTHER REFERENCES (Including Author, Title, Date, Document Pages, Etc.)

VS	Via Etching Process, February 1972	RECEIVED
VS	Multilayer Printed Circuit Board Connections, April 1996	
VS	Process for Forming Copper Clad Vias, August 1989	

EXAMINER	Yuriy Leeeeeebo	DATE CONSIDERED
		APR 8 2002 TC 1700 02/25/2005

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.